Chettinad College of Engineering & Technology, Karur

Department of Electronics and Communication Engineering

News Report

Programme Name: **Four-Day Hands-on Training on "System Verilog for Functional Verification: Concepts to Practice"**

Resource Person:

Mr.V.Govindaraj,

Intel Technology India Private Limited, Bangalore

Internal Resource Person(s) : 1. Ms.D.Ragavi, AP/ECE

2. Mrs.P.Nagarani Sobana, AP/ECE

Date : 30.01.2025 to 02.02.2025 (Four Days)

Venue : DSP & VLSI Laboratory

Number of Participants : 59

Description:

Our Department of Electronics and Communication Engineering successfully conducted a Four Day Value Added Course on **"System Verilog for Functional Verification: Concepts to Practice"** for our III year ECE Students handled by Resource Person Mr.V.Govindaraj, Intel Technology India Private Limited, Bangalore and Internal Faculty Members Ms.D.Ragavi, AP/ECE and Mrs.P.Nagarani Sobana, AP/ECE from 30.01.2025 to 02.02.2025. The course aimed to provide students with fundamental knowledge of digital design and verification methodologies and covered Verilog basics, System Verilog concepts, and hands-on sessions on functional verification.

Day 1: 30.01.2025 (Handled by Mrs.P.Nagarani Sobana, AP/ECE)

The course began with an introduction to Verilog, its basic syntax, signal values, and data types. Students learned about module instantiation, operator usage, and combinational circuit design using Verilog. Tasks were assigned to reinforce these concepts, enabling students to write and execute Verilog programs for logic design.

Day 2: 31.01.2025 (Handled by Ms.D.Ragavi, AP/ECE)

A significant portion of the course focused on testbench development. Topics included module declaration, signal declaration, Design Under Test (DUT) installation, and initializing testbench variables. Time scale and delay systems were also explored to help students understand simulation timing and waveform analysis. Verilog was used for designing and verifying both combinational and sequential circuits through testbench implementation.

Day 3 & 4: 01.02.2025 and 02.02.2025 (Handled by Mr.V.Govindaraj, Intel Technology India Private Limited, Bangalore)

An introduction to verification fundamentals and advanced System Verilog concepts, including Object-Oriented Programming (OOP) and randomization, Inter-Process Communication (IPC) and the use of interfaces to improve modularity and reusability in verification were covered in this session.

Hands-on problem-solving sessions and discussions were conducted to enhance practical understanding. Students designed and verified combinational and sequential circuits, applying functional verification techniques. The course concluded with an assessment of learned skills through assigned tasks, reinforcing the practical aspects of digital design and verification methodologies.

Use Cases done by the Students:

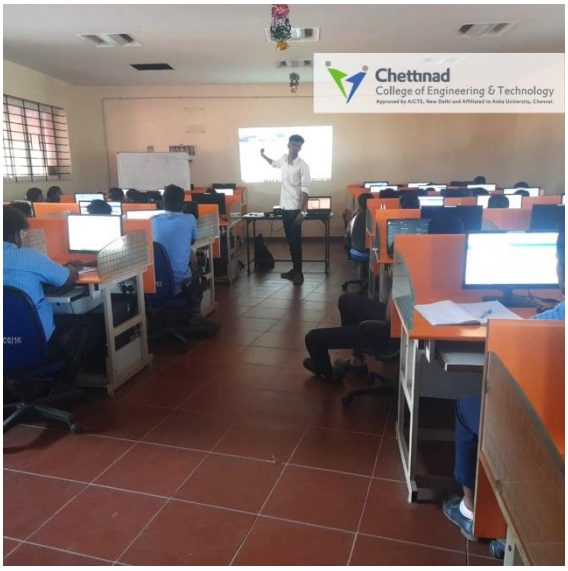
1. Logic Gates and Adder Designs
2. Digital circuits designs
3. 7-Segment Display
4. Traffic Light Controller
5. VEDIC Multiplier
6. Digital Stop Watch
7. Temperature Sensor Design using A/D Conversion

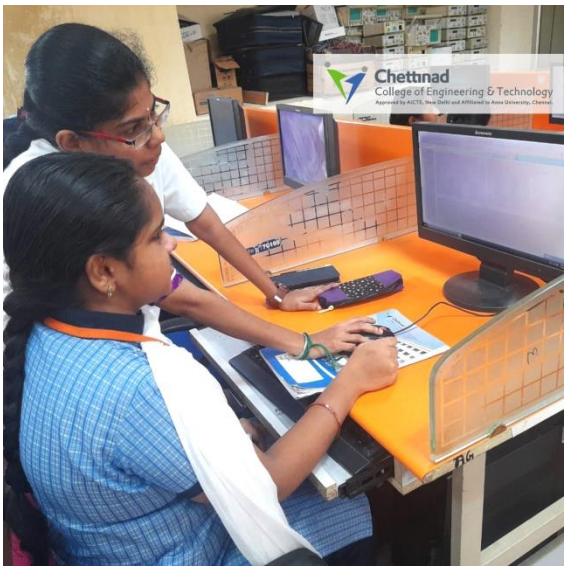
8. Binary to Gray Code Converter

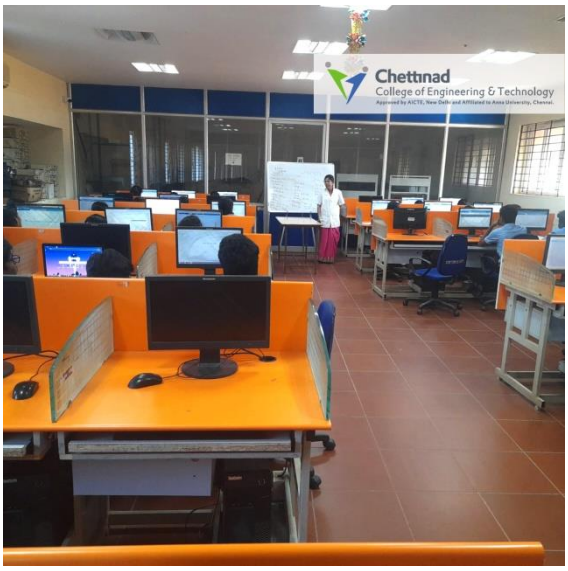
Training Outcomes:

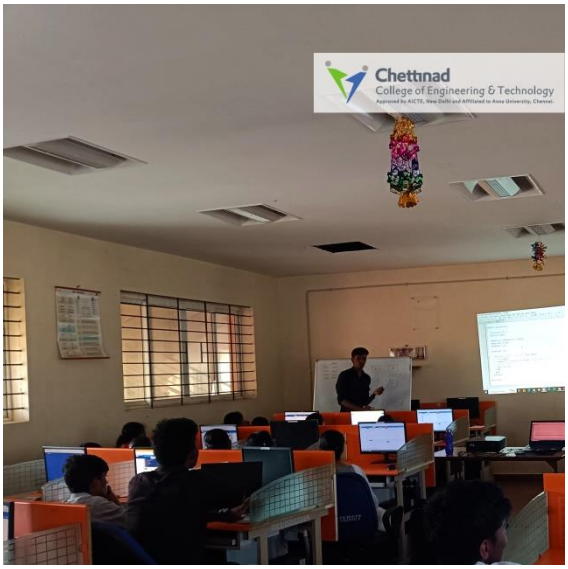
- Students gained proficiency in digital design and functional verification.
- Students developed test benches for verifying circuit functionality.
- Students have enhanced ability to solve digital design and verification challenges.
- Students equipped with fundamental skills required for careers in semiconductor and hardware design industries.

Photos:





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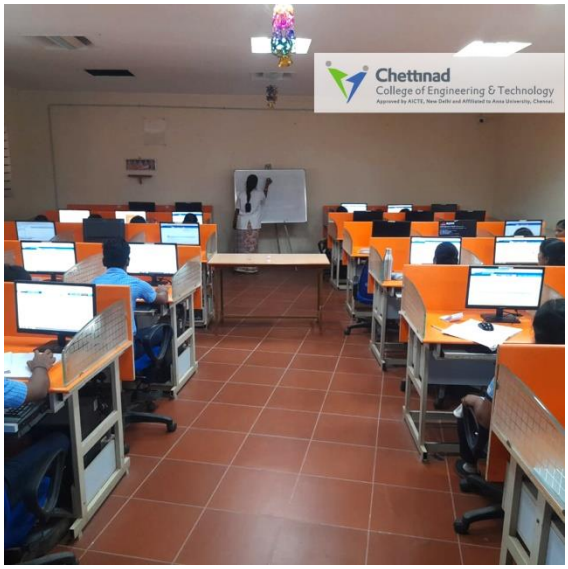
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